Binary Adders

Lecture 6
Section 2.5

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1. Binary Addition
2. Half Adders
3. Full Adders
4. Assignment

Outline

1. Binary Addition
2. Half Adders
3. Full Adders
4. Assignment

Binary Adders

- A half adder (HA) adds two bits and produces a sum bit and a carry bit.
- A full adder (FA) adds two bits and a carry-in bit and produces a sum bit and a carry-out bit.

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A Half Adder

Input		Output	
p	q	sum	carry
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

- Addition of binary digits by a half adder.

A Half Adder

- We see that
  - The sum bit is $p \oplus q$.
  - The carry bit is $p \wedge q$.
- Design circuits for $p \oplus q$ and $p \wedge q$.
- Combine them into a single circuit.

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A Full Adder

Input			Output	
p	q	carry-in	sum	carry-out
1	1	0	0	1
1	0	0	1	0
0	1	0	1	0
0	0	0	0	0
1	1	1	1	1
1	0	1	0	1
0	1	1	0	1
0	0	1	1	0

- Addition of binary digits by a full adder.

A Full Adder

- We can express the sum bit as

$$(p \oplus q) \oplus c_{\text{in}} = p \oplus q \oplus c_{\text{in}}$$

  and the carry-out c_{out} as

$$(p \wedge q) \vee ((p \oplus q) \wedge c_{\text{in}}).$$

- We can implement these two expressions in a circuit.

A Full Adder

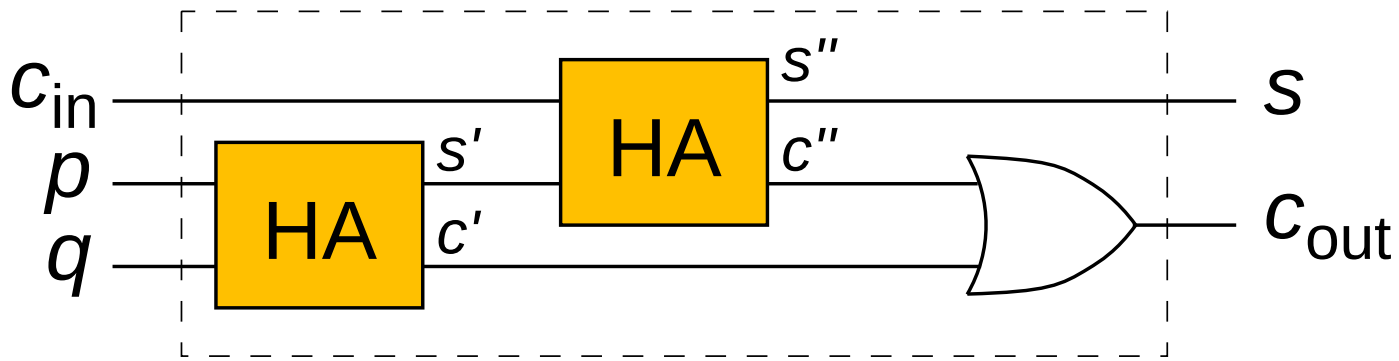
- Use a HA to add p and q. This produces

$$s' = p \oplus q.$$
$$c' = p \wedge q.$$

- Then use another HA to add c_{in} to s' to get the final sum and carry-out bits.

$$s = s' \oplus c_{\text{in}}.$$
$$c_{\text{out}} = c' \vee (s' \wedge c_{\text{in}}).$$

Circuits



Circuits

- Design a circuit for a full adder using two half adders.
- Design a circuit for an 8-bit adder using 8 full adders.

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- Read Section 2.5, pages 78 - 84.
- Exercises 1, 2, 7, 8, 13, 14, 17, 18, 21, page 94.